WHAT IS CLAIMED IS:

1. An antifuse comprising:

a well of a first conductivity type in a substrate of a second conductivity type;

a first conductive terminal of the second conductivity type; and

an insulator between the well and the first conductive terminal.

2. The antifuse of claim 1, further comprising an ohmic contact in the well as a second conductive terminal.

3. The antifuse of claim 2 wherein:

the substrate comprises a p-type silicon substrate;

the well comprises an n-type well in the substrate;

the ohmic contact comprises an n+-type diffusion region;

the insulator comprises a layer of oxide; and

the first conductive terminal comprises a layer of p-type polysilicon.

4. The antifuse of claim 2 wherein:

the substrate comprises an n-type silicon substrate;

the well comprises a p-type well in the substrate;

the ohmic contact comprises a p+-type diffusion region;

the insulator comprises a layer of oxide; and

the first conductive terminal comprises a layer of n-type polysilicon.

5. An integrated circuit comprising:

a first circuit;

a second circuit; and

an antifuse coupled between the first circuit and the second circuit, the antifuse comprising:

a well of a first conductivity type in a substrate of a second conductivity type;

a first conductive terminal of the second conductivity type; and

an insulator between the well and the first conductive terminal.

6. The integrated circuit of claim 5, further comprising an ohmic contact in the well as a second conductive terminal.

7. The integrated circuit of claim 6 wherein:

the substrate comprises a p-type silicon substrate;

the well comprises an n-type well in the substrate;

the ohmic contact comprises an n+-type diffusion region;

the insulator comprises a layer of oxide;

the first conductive terminal comprises a layer of p-type polysilicon;

the first circuit comprises a programming logic circuit; and

the second circuit comprises an external pin and a bias circuit.

8. The integrated circuit of claim 6 wherein:

the substrate comprises an n-type silicon substrate;

the well comprises a p-type well in the substrate;

the ohmic contact comprises a p+-type diffusion region;

the insulator comprises a layer of oxide;

the first conductive terminal comprises a layer of n-type polysilicon;

the first circuit comprises a programming logic circuit; and

the second circuit comprises an external pin and a bias circuit.

9. The integrated circuit of claim 5 wherein the integrated circuit comprises a memory device and further comprises an array of memory cells, an address decoder, a plurality of input/output paths, and an input/output control circuit.

10. An integrated circuit comprising:

a programming logic circuit;

an external pin; and

a plurality of antifuses, each antifuse comprising:

a well of a first conductivity type in a substrate of a second conductivity type, the well being coupled to the external pin;

a first conductive terminal of the second conductivity type coupled to the programming logic circuit; and

an insulator between the well and the first conductive terminal.

11. The integrated circuit of claim 10, further comprising an ohmic contact in the well coupled to the external pin.

12. The integrated circuit of claim 11 wherein:

the substrate comprises a p-type silicon substrate;

the well comprises an n-type well in the substrate;

the ohmic contact comprises an n+-type diffusion region;

the insulator comprises a layer of oxide; and

the first conductive terminal comprises a layer of p-type polysilicon.

13. The integrated circuit of claim 11 wherein:

the substrate comprises an n-type silicon substrate;

the well comprises a p-type well in the substrate;

the ohmic contact comprises a p+-type diffusion region;

the insulator comprises a layer of oxide; and

the first conductive terminal comprises a layer of n-type polysilicon.

14. The integrated circuit of claim 10 wherein the integrated circuit comprises a memory device and further comprises an array of memory cells, an address decoder, a plurality of input/output paths, and an input/output control circuit.

15. An antifuse bank comprising:

a programming logic circuit;

an external pin; and

a plurality of antifuses, each antifuse comprising:

a well of a first conductivity type in a substrate of a second conductivity type, the well being coupled to the external pin;

a first conductive terminal of the second conductivity type coupled to the programming logic circuit; and

an insulator between the well and the first conductive terminal.

16. The antifuse bank of claim 15, further comprising an ohmic contact in the well coupled to the external pin.

17. The antifuse bank of claim 16 wherein:

the substrate comprises a p-type silicon substrate;

the well comprises an n-type well in the substrate;

the ohmic contact comprises an n+-type diffusion region;

the insulator comprises a layer of oxide; and

the first conductive terminal comprises a layer of p-type polysilicon.

18. The antifuse bank of claim 16 wherein:

the substrate comprises an n-type silicon substrate;

the well comprises a p-type well in the substrate;

the ohmic contact comprises a p+-type diffusion region;

the insulator comprises a layer of oxide; and

the first conductive terminal comprises a layer of n-type polysilicon.

19. A memory device comprising:

an array of memory cells;

an address decoder;

a plurality of input/output paths;

an input/output control circuit; and

an antifuse bank comprising:

a programming logic circuit;

an external pin; and

a plurality of antifuses, each antifuse comprising:

a well of a first conductivity type in a substrate of a second conductivity type, the well being coupled to the external pin;

a first conductive terminal of the second conductivity type coupled to the programming logic circuit; and

an insulator between the well and the first conductive terminal.

20. The memory device of claim 19, further comprising an ohmic contact in the well coupled to the external pin.

21. The memory device of claim 20 wherein:

the substrate comprises a p-type silicon substrate;

the well comprises an n-type well in the substrate;

the ohmic contact comprises an n+-type diffusion region;

the insulator comprises a layer of oxide; and

the first conductive terminal comprises a layer of p-type polysilicon.

22. The memory device of claim 20 wherein:

the substrate comprises an n-type silicon substrate;

the well comprises a p-type well in the substrate;
the ohmic contact comprises a p+-type diffusion region;
the insulator comprises a layer of oxide; and
the first conductive terminal comprises a layer of n-type polysilicon.

23. An integrated circuit comprising:
a circuit;
a plurality of antifuses, each antifuse comprising a first conductive terminal of a first conductivity type coupled to the circuit to receive a first programming voltage, and a well of a second conductivity type in a substrate of the first conductivity type; and
an external pin in the integrated circuit coupled to the well of each antifuse to receive a second programming voltage.

24. The integrated circuit of claim 23, further comprising an ohmic contact in the well of each antifuse coupled to the external pin.

25. The integrated circuit of claim 24 wherein:
the circuit comprises a programming logic circuit;
the substrate comprises a p-type silicon substrate;
the well comprises an n-type well in the substrate;
the ohmic contact comprises an n+-type diffusion region;

the insulator comprises a layer of oxide; and
the first conductive terminal comprises a layer of p-type polysilicon.

26. The integrated circuit of claim 24 wherein:
the circuit comprises a programming logic circuit;
the substrate comprises an n-type silicon substrate;
the well comprises a p-type well in the substrate;

the ohmic contact comprises a p+-type diffusion region;

the insulator comprises a layer of oxide; and

the first conductive terminal comprises a layer of n-type polysilicon.

27. A method comprising:

coupling a first programming voltage to a well of a first conductivity type in a substrate of a second conductivity type in an antifuse; and

coupling a second programming voltage to a conductive terminal of the second conductivity type in the antifuse to create a current path through an insulator between the conductive terminal and the well to program the antifuse.

28. The method of claim 27 wherein coupling a first programming voltage comprises coupling a first programming voltage to an ohmic contact in the well of the first conductivity type in the substrate of the second conductivity type in the antifuse.

29. The method of claim 28 wherein:

coupling a first programming voltage comprises coupling a very high positive voltage to an n+-type diffusion region in an n-type well in a p-type substrate in an antifuse; and

coupling a second programming voltage comprises coupling a ground voltage reference to a layer of p-type polysilicon in the antifuse to create a current path through an insulating layer of oxide between the layer of p-type polysilicon and the n-type well to program the antifuse.

30. The method of claim 28 wherein:

coupling a first programming voltage comprises coupling a very negative voltage to a p+-type diffusion region in an p-type well in an n-type substrate in an antifuse; and

coupling a second programming voltage comprises coupling a supply voltage to a layer of n-type polysilicon in the antifuse to create a current path through an insulating

layer of oxide between the layer of n-type polysilicon and the p-type well to program the antifuse.

31. A method of operating an integrated circuit comprising:

selecting an antifuse coupled between a first circuit and a second circuit in an integrated circuit;

coupling a first programming voltage to a well of a first conductivity type in a substrate of a second conductivity type in the selected antifuse; and

coupling a second programming voltage to a conductive terminal of the second conductivity type in the selected antifuse to create a current path through an insulator between the conductive terminal and the well to program the selected antifuse.

32. The method of claim 31 wherein coupling a first programming voltage comprises coupling a first programming voltage to an ohmic contact in the well of the first conductivity type in the substrate of the second conductivity type in the selected antifuse.

33. The method of claim 32 wherein:

selecting an antifuse comprises selecting an antifuse from a plurality of antifuses coupled between a programming logic circuit and an external pin coupled to a bias circuit in the integrated circuit;

coupling a first programming voltage comprises coupling a very high positive voltage to the external pin that is coupled to an n+-type diffusion region in an n-type well in a p-type substrate in the selected antifuse; and

coupling a second programming voltage comprises coupling a ground voltage reference from the programming logic circuit to a layer of p-type polysilicon in the selected antifuse to create a current path through an insulating layer of oxide between the layer of p-type polysilicon and the n-type well to program the selected antifuse.

34. The method of claim 32 wherein:

selecting an antifuse comprises selecting an antifuse from a plurality of antifuses coupled between a programming logic circuit and an external pin coupled to a bias circuit in the integrated circuit;

coupling a first programming voltage comprises coupling a very negative voltage to the external pin that is coupled to a p+-type diffusion region in a p-type well in an n-type substrate in the selected antifuse; and

coupling a second programming voltage comprises coupling a supply voltage from the programming logic circuit to a layer of n-type polysilicon in the selected antifuse to create a current path through an insulating layer of oxide between the layer of n-type polysilicon and the p-type well to program the selected antifuse.

35. A method of operating an integrated circuit comprising:

selecting an antifuse coupled between a circuit and an external pin in the integrated circuit;

coupling a first programming voltage to the external pin that is coupled to a well of a first conductivity type in a substrate of a second conductivity type in the selected antifuse; and

coupling a second programming voltage from the circuit to a conductive terminal of the second conductivity type in the selected antifuse to create a current path through an insulator between the conductive terminal and the well to program the selected antifuse.

36. The method of claim 35 wherein coupling a first programming voltage comprises coupling a first programming voltage to the external pin that is coupled to an ohmic contact in the well of the first conductivity type in the substrate of the second conductivity type in the selected antifuse.

37. The method of claim 36 wherein:

selecting an antifuse comprises selecting an antifuse from a plurality of antifuses coupled between a programming logic circuit and the external pin coupled to a bias circuit in the integrated circuit;

coupling a first programming voltage comprises coupling a very high positive voltage to the external pin that is coupled to an n+-type diffusion region in an n-type well in a p-type substrate in the selected antifuse; and

coupling a second programming voltage comprises coupling a ground voltage reference from the programming logic circuit to a layer of p-type polysilicon in the selected antifuse to create a current path through an insulating layer of oxide between the layer of p-type polysilicon and the n-type well to program the selected antifuse.

38. The method of claim 36 wherein:

selecting an antifuse comprises selecting an antifuse from a plurality of antifuses coupled between a programming logic circuit and the external pin coupled to a bias circuit in the integrated circuit;

coupling a first programming voltage comprises coupling a very negative voltage to the external pin that is coupled to a p+-type diffusion region in a p-type well in an n-type substrate in the selected antifuse; and

coupling a second programming voltage comprises coupling a supply voltage from the programming logic circuit to a layer of n-type polysilicon in the selected antifuse to create a current path through an insulating layer of oxide between the layer of n-type polysilicon and the p-type well to program the selected antifuse.

39. A method comprising:

selecting circuits in a system to be coupled together;

programming an antifuse in the system to couple two or more of the selected circuits together, comprising:

coupling a first programming voltage to a well of a first conductivity type in a substrate of a second conductivity type in the antifuse; and

coupling a second programming voltage to a conductive terminal of the second conductivity type in the antifuse to create a current path through an insulator between the conductive terminal and the well to program the antifuse.

40. The method of claim 39 wherein coupling a first programming voltage comprises coupling a first programming voltage to an ohmic contact in the well of the first conductivity type in the substrate of the second conductivity type in the antifuse.

41. The method of claim 40 wherein:

coupling a first programming voltage comprises coupling a very high positive voltage to an n+-type diffusion region in an n-type well in a p-type substrate in the antifuse; and

coupling a second programming voltage comprises coupling a ground voltage reference to a layer of p-type polysilicon in the antifuse to create a current path through an insulating layer of oxide between the layer of p-type polysilicon and the n-type well to program the antifuse.

42. The method of claim 40 wherein:

coupling a first programming voltage comprises coupling a very negative voltage to a p+-type diffusion region in an p-type well in an n-type substrate in the antifuse; and

coupling a second programming voltage comprises coupling a supply voltage to a layer of n-type polysilicon in the antifuse to create a current path through an insulating layer of oxide between the layer of n-type polysilicon and the p-type well to program the antifuse.

43. A method of forming an antifuse comprising:

forming a well of a first conductivity type in a substrate of a second conductivity type;

forming an insulator over the well; and

forming a first conductive terminal of the second conductivity type over the insulator.

44. The method of claim 43, further comprising forming an ohmic contact in the well as a second conductive terminal.

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45. The method of claim 43 wherein:

forming a well comprises forming an n-type well in a p-type silicon substrate and further comprises:

forming an n+-type diffusion region in the well;

forming an n+-type drain diffusion region in the well;

forming an n+-type source diffusion region in the well;

forming an insulator comprises forming a layer of oxide over the well between the drain diffusion region and the source diffusion region; and

forming a first conductive terminal comprises forming a p-type polysilicon gate electrode over the layer of oxide.

46. The method of claim 43 wherein:

forming a well comprises forming a p-type well in an n-type silicon substrate and further comprises:

forming a p+-type diffusion region in the well;

forming a p+-type drain diffusion region in the well;

forming a p+-type source diffusion region in the well;

forming an insulator comprises forming a layer of oxide over the well between the drain diffusion region and the source diffusion region; and

forming a first conductive terminal comprises forming an n-type polysilicon gate electrode over the layer of oxide.

47. An antifuse comprising:

a body isolated by an isolation insulator;

a conductive terminal; and

a gate insulator between the body and the first conductive terminal.

48. The antifuse of claim 47, further comprising:

an ohmic contact in the body; and

wherein the body comprises silicon isolated by the isolation insulator.

49. The antifuse of claim 48 wherein:

the body comprises n-type silicon;

the ohmic contact comprises an n+-type diffusion region in the body;

the isolation insulator comprises a shallow trench isolation insulator comprising oxide and further comprises a layer of SOI oxide between the body and a silicon substrate;

the gate insulator comprises a layer of oxide; and

the conductive terminal comprises a layer of n+-type polysilicon.

50. The antifuse of claim 48 wherein:

the body comprises p-type silicon;

the ohmic contact comprises a p+-type diffusion region in the body;

the isolation insulator comprises a shallow trench isolation insulator comprising oxide and further comprises a layer of SOI oxide between the body and a silicon substrate;

the gate insulator comprises a layer of oxide; and

the conductive terminal comprises a layer of p+-type polysilicon.

51. The antifuse of claim 48 wherein:

the body comprises n-type silicon;

the ohmic contact comprises an n+-type diffusion region in the body;

the isolation insulator comprises a shallow trench isolation insulator comprising oxide and further comprises a layer of SOI oxide between the body and a silicon substrate;

the gate insulator comprises a layer of oxide; and

the conductive terminal comprises a layer of p+-type polysilicon.

52. The antifuse of claim 48 wherein:

the body comprises p-type silicon;

the ohmic contact comprises a p+-type diffusion region in the body;

the isolation insulator comprises a shallow trench isolation insulator comprising oxide and further comprises a layer of SOI oxide between the body and a silicon substrate;

the gate insulator comprises a layer of oxide; and

the conductive terminal comprises a layer of n+-type polysilicon.